

A TEMPERATURE ANALYSIS OF HIGH-POWER ALGaN/GaN HEMTS

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ABSTRACT

Galliumnitride (GaN) has become a strategic superior material for space, defense and civil applications, primarily for power amplification at RF and mm-wave frequencies. For AlGaN/GaN high electron mobility transistors (HEMT), an outstanding performance combined together with low cost and high flexibility can be obtained using a System-in-a-Package (SIP) approach. Since thermal management is extremely important for these high power applications, a hybrid integration of the HEMT onto an AlN carrier substrate is proposed. In this study we investigate the temperature performance for AlGaN/GaN HEMTs integrated onto AlN using flip-chip mounting. Therefore, we use thermal simulations in combination with experimental results using micro-Raman spectroscopy and electrical dc-analysis.

1. INTRODUCTION

The AlGaN/GaN material system has many advantages for high power RF applications [1]. It combines a higher output power density (even at high frequency), a higher output impedance (easier matching), a larger bandwidth and better linearity than other existing technologies (like Si-LDMOS or GaAs p-HEMT). These features follow directly from the physical properties of GaN: the large bandgap ($E_g = 3.4$ eV) results in a breakdown electrical field ten times larger than Si. This allows transistor operation at high bias voltage (>50 V). Moreover it is possible to engineer piezoelectric AlGaN/GaN heterostructures, with spontaneous formation of a two-dimensional electron gas (2DEG), exhibiting high electron mobility and high current density, combined with high electron saturation velocity.

The AlGaN/GaN heterostructures are usually grown on sapphire, SiC and recently also on Si substrates. Sapphire substrates have the advantage of low cost, however, for realizing high power applications their low thermal conductivity ($k = 35$ W/m.K) compared to e.g. SiC ($k = 400$ W/m.K) is a major drawback. To overcome

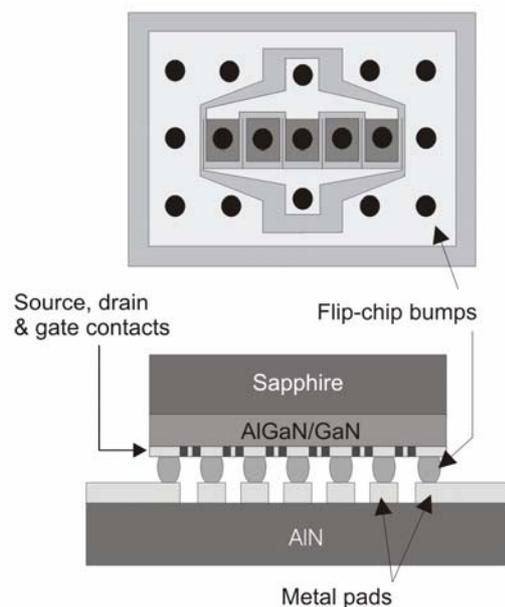


Fig.1: Top view and cross-section of the flip-chip bump design: bumps are placed directly on the source and drain ohmic contacts. In this way, there is a direct thermal and electrical contact between the ohmic contacts and the metal pads on the AlN carrier.

the low thermal conductivity of sapphire, flip-chip bumps can be used to interconnect the HEMT both electrically and thermally to a AlN carrier [2]. By integrating passive components onto the AlN, using a Multi-Chip-Module technology a System-in-a-Package (SIP) integration is obtained. In this paper we will study a new flip-chip bump design, to achieve a good thermal performance. We will compare finite element thermal simulations to experimental results, using electrical DC-characterization, and micro-Raman spectroscopy. We will demonstrate that using the novel bump design an improved thermal performance for multi-finger HEMTs on sapphire substrates can be achieved.

2. FABRICATION

The AlGaIn/GaN heterostructures used in this work were grown by metal-organic vapor phase epitaxy (MOVPE) on sapphire substrates. On top of the AlGaIn, an in-situ 3.5 nm Si₃N₄ passivation layer is grown. This Si₃N₄ layer enhances the electrical performance of the device, reduces the dispersion effects, and protects the surface during processing [3]. The HEMTs are fabricated using a 5-step process: mesa etching, ohmic contact formation, gate and contact metal deposition and passivation. The gate length L_g is 1.5 μm , and the width of a single gate finger $W_g = 100 \mu\text{m}$. The distance between two neighboring gate fingers is 100 μm .

To lower the device temperature, we integrated the HEMT onto a AlN carrier substrate using flip-chip bumps. In our new flip-chip bump design, bumps are placed both on source and drain contacts of the HEMT (see Fig.1). More details about the flip-chip bump design can be found in [4]. On the AlN substrate, metal contact pads are deposited by electroplating. Note that AlN is here the preferred carrier substrate, because of its high thermal conductivity and low substrate loss at RF frequencies.

TABLE I

THERMAL CONDUCTIVITIES USED IN THE SIMULATIONS

Material	Thermal conductivity [W/m.K]
GaN	160.(300 K/T) ^{1.4}
Sapphire	35.(300 K/T)
Au	310
AlN	180.(300 K/T) ^{1.4}
Solder bumps	50

3. THERMAL SIMULATIONS

To study the thermal behavior of the HEMT device for the different integration structures, a fully three dimensional finite element model is used [5]. Heat sources are defined between the ohmic contact regions of the multiple gate-finger HEMT. The heat generation is assumed to be uniform within these heat sources. For the simulations a constant temperature at the backside of the AlN carrier ($T = 25 \text{ }^\circ\text{C}$) is defined as a boundary condition. The thermal conductivities of the materials used in the simulations are given in Table 1. For GaN, sapphire, and AlN, the temperature dependency of the thermal conductivity is taken into account with a temperature dependence as given in Table I.

Fig. 2 displays a cross-section of the temperature distribution within the HEMT after flip-chip integration,

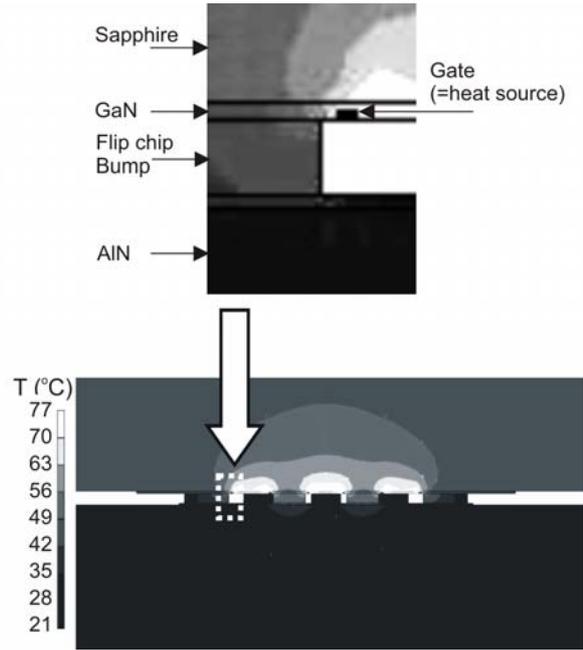


Fig.2: Temperature distribution simulation (cross-section) of a HEMT on sapphire after flip-chip, at a power dissipation of 3 W/mm.

for a total power dissipation of 1.8 W. Since the total gate width of the HEMT $W_g = 0.6 \text{ mm}$, this corresponds to a dissipated power density of 3 W/mm. From the simulations, we find a maximum temperature $T_{max} = 77 \text{ }^\circ\text{C}$, which is much lower compared to a HEMT on sapphire before integration ($T_{max} = 169^\circ\text{C}$). From the figure it is very clear that the flip-chip bumps act as effective heat sinks. As a comparison, also a HEMT on SiC was simulated: since SiC has a much higher thermal conductivity, a lower maximum temperature was obtained: $T_{max} = 46 \text{ }^\circ\text{C}$. Nevertheless, this result shows that the thermal performance of the HEMT on sapphire after flip-chip becomes quite close to the HEMT on SiC, and at the same time it has the advantage of a much lower substrate cost.

4. EXPERIMENTAL RESULTS

DC-measurements and micro-Raman spectroscopy were used to assess the impact of flip-chip integration on the thermal performance of the HEMT. When a high drain-source voltage V_{ds} is applied, the 2-DEG saturation current $I_{ds,sat}$ will decrease due to the self-heating effect. From this decrease (ΔI_{sat}), it is possible to extract the temperature of the active region [6]:

$$\Delta I_{sat} = -g_m (I_{sat} \cdot \Delta R_s + \Delta V_T) \quad (1)$$

In this equation, ΔR_s and ΔV_T represent the change of source resistance and the change of threshold voltage compared to their reference value at room temperature,

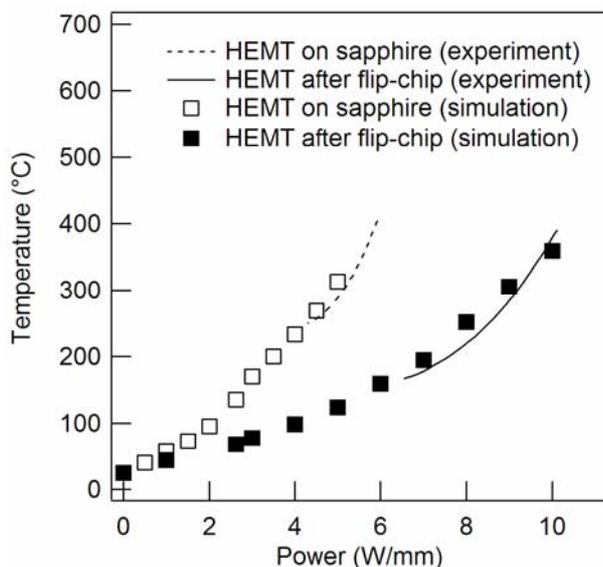


Fig.3: Temperature versus power for a HEMT on sapphire before and after flip-chip, obtained both from simulations and electrical measurements.

respectively. The dependencies $V_T = f(T)$ and $R_s = f(T)$ were determined experimentally, using an external heating source to heat the devices up to constant temperature. As a result, the channel temperature versus dissipated power is obtained (see Fig. 3). From this figure it is clear that the flip-chip integration improves the thermal performance of the HEMT. Moreover there is a good agreement between the measured and simulated temperatures.

In order to measure experimentally the temperature distribution within the HEMT, an integrated Raman-IR system was used. This system consists of a Renishaw InVia Raman microscope equipped with motorized XY positioning stage and a QFI IR thermal microscope, switchable between Raman and IR detection modes. The 488nm line of an Argon ion laser was employed as excitation source for the Raman measurements. Raman shift of the E_2 phonon of GaN was probed to determine the temperature of powered devices. More details of the experimental set-up can be found in [7-8]. As the sapphire substrate was double-side polished, device temperature could be measured through the substrate. As a result, device temperature was accessible not only in the source drain openings, but also directly underneath the contacts and where the flip-chip tin bumps are located, which is a major advantage [9]. Fig. 4 displays an obtained linescan together with the thermal simulation showing that there is an excellent agreement between both obtained results. Note that peak temperatures determined from electrical device analysis (Fig. 3) are slightly smaller compared to peak temperatures obtained

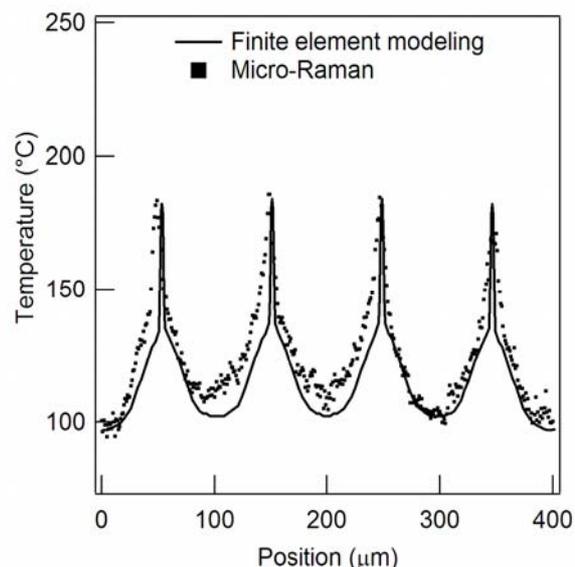


Fig.4: Temperature linescan of a HEMT on sapphire after flip-chip integration, at a dissipated power of 6.8 W/mm. Micro-Raman spectroscopy and finite element simulations are compared.

from the Raman measurements, possibly indicating that the electrical device characterization technique determines not peak device temperature, but a slightly lower average temperature.

5. CONCLUSION

We have investigated the temperature distribution in high-power AlGaIn/GaN HEMTs before and after flip-chip, with thermal simulations, electrical and micro-Raman analysis. We obtained an excellent agreement between simulation and experimental results. We have shown that by using our new flip-chip design, with bumps on the source and drain ohmic contacts, a much better thermal performance is obtained, because the flip-chip bumps, which are very close to the active device area, act as very effective heat sinks.

6. ACKNOWLEDGEMENTS

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