DTIP of MEMS & MOEMS Stresa, Italy, 26-28 April 2006

CAPACITIVE TEST-STRUCTURES DESIGN METHODOLOGY FOR THE EXTRACTION OF AIR-GAP AND DIELECTRIC THICKNESS OF A MEMS PROCESS

Marco Bellei[1], Benno Margesin[2], Roberto Gaddi[1], Antonio Gnudi[1], Flavio Giacomozzi[2]

[1]ARCES-DEIS, University of Bologna, Viale Risorgimento 2, 40125 Bologna, Italy
tel: +39 051 2093049, fax: +39 051 2093779, corr. author e-mail: mbellei@deis.unibo.it
[2] Istituto Trentino di Cultura ITC-irst, Via Sommarive 18, 38050 Povo (TN), Italy

ABSTRACT

The air-gap and dielectric thicknesses are key technology parameters of a micromachining fabrication process; their correct estimation is necessary for both good prediction of MEMS devices behavior and process monitoring. In this paper we present a methodology for their accurate quantification making use of capacitive test-structures, in order to allow automated data-extraction or, in general, capacitance measurements with standard lab instrumentation; the parameters are computed from measurements through a simple analytical model.

Model validation and robustness to main parameters deviations and undesired mechanical effects are investigated by finite element analysis using CoventorWare™.

1. INTRODUCTION

The behavior of MEMS devices fabricated with surface micromachining process is generally influenced by the vertical distance between the suspended structure and the underlying layer (air-gap) and by the thickness of dielectric layers if employed in functional parts of the device. From a technological point of view, the air-gap is the local thickness of the sacrificial layer and thus its value is fixed by technology. Especially in designs with out-of-plane movement of suspended parts, the designer needs to know the air-gap value for accurate devices behavior prediction; for example, the pull-in voltage, the RF performances of switches, the capacitance ratio of varactors [1], the electromechanical excitation in resonating structures [2], the damping phenomena [3] and the switching time [4] can be strongly influenced by the air-gap value. The thickness value of dielectric layers can be also necessary for behavior prediction of purely capacitive structures. Besides, the knowledge of the deposited layers thickness is a key aspect for post-fabrication process monitoring.

Although profilometry (both stylus and optical), interferometry and ellipsometry measurements are very accurate for those purposes, usually they are not suited for automatic measurements and they need dedicated expensive instrumentation.

In the present work, we introduce a set of capacitive test-structures for thickness extraction of the above-mentioned layers; design aspects and preliminary results will be presented.

2. METHODOLOGY AND MODEL FOR PARAMETERS EXTRACTION

The employed methodology for the thickness extraction of the sacrificial and dielectric layers is based on a parallel-plates capacitance taking into account also parasitic contributions [5]. Two geometrical configurations are interesting for our purposes: a standard Metal-Insulator-Metal (fig.1-d) and a crossed-lines capacitor (fig. 1-a, b, c). Taking into account all the capacitive effects defined in figure 1, the total capacitance can be respectively expressed as:

$$C_{MIM} = C_A + C_P$$

$$C_{CrL} = C_A + C_{SL} + C_{LS} + 4C_{CR}$$

where C_A is the area capacitance of an ideal parallel-plate capacitor; C_P is the perimeter capacitance due to edge-to-edge effects; C_{SL} and C_{LS} are due to the edge-to-plane effects; C_{CR} is the edge-to-edge capacitance due to cross effect of the lines outside the overlapping region.

For a MIM capacitor we assume

$$C_A = C_A^{SP} A, \quad C_A^{SP} = \varepsilon / T \qquad (1)$$

$$C_P = C_P^{SP} P$$

where $A = W_L W_S$ and $P = 2(W_L + W_S)$ are respectively the area and perimeter of the MIM plates; ε is the absolute permittivity of the medium between the conductors; T is their distance; C_A^{SP} and C_P^{SP} are the specific area and perimeter capacitances.

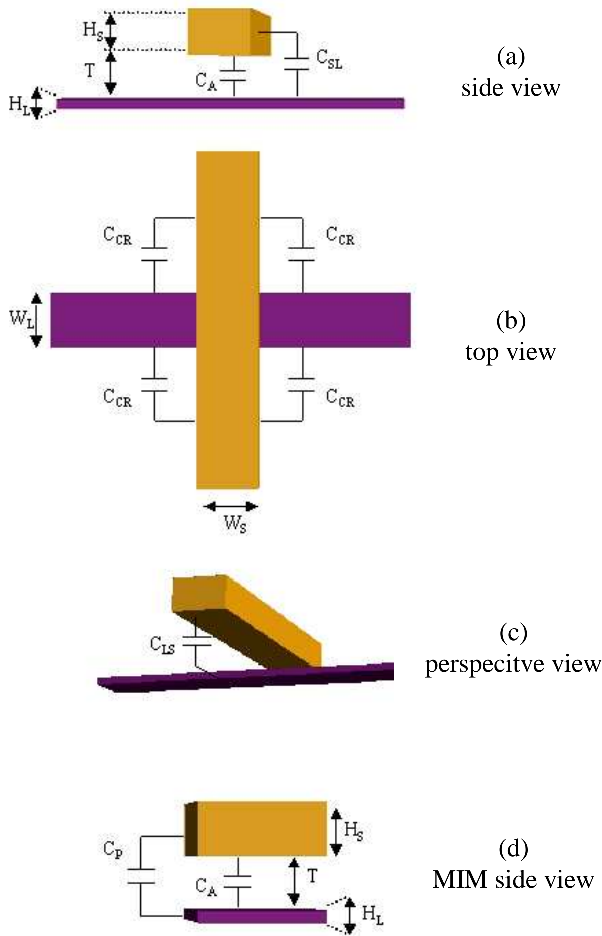

Figure 1 Geometrical parameters and capacitance definitions for two crossing lines (different views: a, b, c) and for a standard parallel plates capacitor (d).

For the crossed-lines configuration, if A is the overlapping area, we assume the expression (1) for C_A; moreover

$$C_{SL} = C_{SL}^{SP}\, 2W_L$$

$$C_{LS} = C_{LS}^{SP}\, 2W_S.$$

If the conductors thicknesses H_L and H_S are comparable or T is not too small, we can also assume

$$C_{LS}^{SP} \approx C_{SL}^{SP} \equiv C_P^{SP} \quad (2)$$

so that

$$C_{SL} + C_{LS} = C_P^{SP}\, 2(W_L + W_S)$$

where $2(W_L + W_S)$ is the overlapping perimeter P.

In both configurations, if we vary only W_L and W_S while maintaining the perimeter P constant (maintaining constant also H_L, H_S, T), we can write the general expression for capacitance:

$$C(A) = C_A^{SP} A + C_O \quad (3)$$

where C_O is a constant which summarizes all other contributions.

Thus, from a linear regression on a set of at least three capacitance values vs. nominal area, designed in order to have constant perimeter, we can extract C_A^{SP} and check the error on the assumptions of the model. Finally, the thickness T is computed by (1), if ε is known.

3. DIELECTRIC THICKNESS EXTRACTION

Figure 2 shows the fabricated Metal-Insulator-Metal capacitor bank for dielectric thickness extraction. The insulating layer is a low temperature oxide; for further details on fabrication refer to [6].

This bank includes five capacitors with the same perimeter but different area. By capacitive measurements on a set of eight identical banks scattered on the same wafer, we have obtained the graph shown in figure 3. From linear regression on the data points, it is possible to extract C_A^{SP} that corresponds to the angular coefficient of the interpolating line expressed by (3); finally the dielectric thickness is computed, by assuming the knowledge of the dielectric constant of the insulating layer, as described in the previous paragraph. The parasitic capacitances due to the pads and the systematic errors due to measurement setup, do not affect the results because they can be assumed constant and so they are included in the C_O parameter. The extracted value of the unit area capacitance is $C_A^{SP}=(73\pm1.1)10^{-5}$ F/m^2.

The accuracy is limited by the knowledge of the dielectric constant. By assuming the nominal value $\varepsilon_r=4$ for the insulating layer, one obtains the thickness T=49±1 nm, that is in agreement with the value measured by interferometry technique.

The same technique can be used to extract the dielectric constant if the thickness is well known by other techniques.

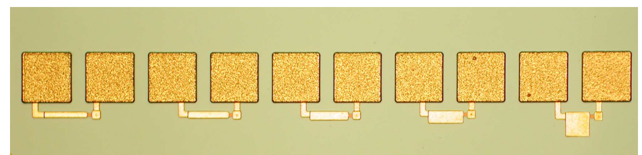

Figure 2 Optical image of the fabricated MIM capacitors bank, featuring variable area and constant perimeter.

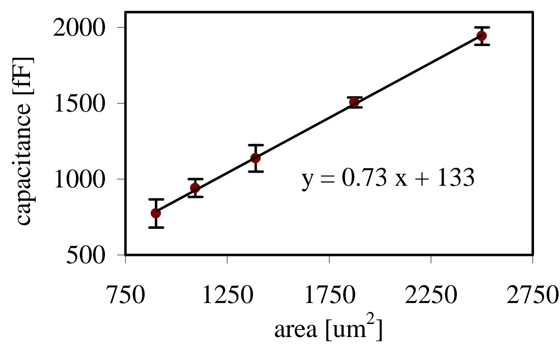

Figure 3 Measured MIM capacitances versus nominal area and linear regression (the error bars are the measurement standard deviation).

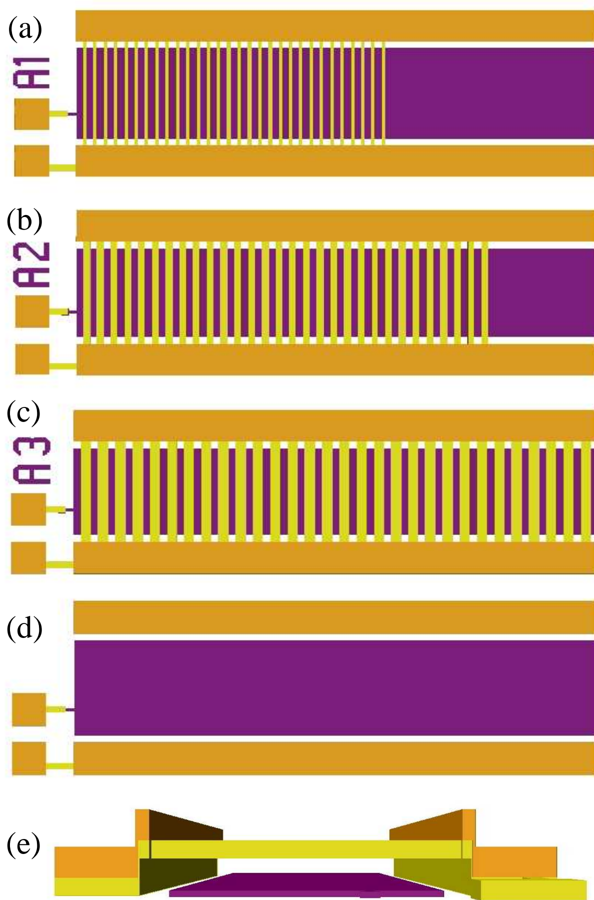

Figure 4 Layout images of the constant perimeter-variable area capacitors, designed for air-gap extraction (a, b, c), supporting structure (d) and cross section view of the above-mentioned capacitors (e).

4. AIR-GAP EXTRACTION

The design for air-gap extraction is more complicated with respect to MIM capacitors, since the suspended plates generally need etch holes for structure release. This can introduce a relevant error on the capacitive analytical model (3); moreover, the design of the plates for capacitors with constant perimeter and variable area becomes cumbersome when taking into account the holes area and perimeter.

Thus, the first design issue was to avoid etch holes so that maximum width of suspended plate is limited by technology design rules through lateral depth etching; in order to maintain good accuracy, it is also necessary to measure a relatively high capacitance, so we have employed a large number of parallel connected narrow beams. Layout image of the capacitors bank is shown in figure 4. The use of narrow beams is also necessary in order to neglect the common mechanical transverse curling that limits the extraction accuracy. Observe that the geometry of the supporting structure and of the bottom electrode (fig. 4-d) is almost the same for all capacitors and this introduces a nearly constant parasitic capacitance.

Since every suspended beam crosses the underlying central electrode and the distance between neighboring beams is much higher than T, each capacitance can be described with a crossing lines model. The total number N_S of suspended beams is the same for all the three capacitors, in order to simplify the design and to have a constant total cross capacitance $N_S C_{CR}$. The total overlapping area and perimeter become respectively $A=A_B N_S$ and $P=P_B N_S$, where A_B and P_B are the area and the perimeter of each beam.

Figure 5 shows the finite element (FE) capacitance simulation results for different values of the air-gap using the parameters listed in table 1. From linear regression, as described in the previous paragraphs, we have then computed the specific area capacitance and subsequently the air-gap. Relative percentage error between the extracted air-gap and the nominal air-gap imposed in the FE simulations is shown in figure 6. The error is mainly due to the assumption that the overlap area contributing to C_A is independent from the air-gap.

Since our fabrication process allows multiple choice for the thickness H_S of the suspended beams, we checked the robustness of the model for lower and higher thicknesses, using the nominal value of 3 um for the air-gap. Extraction from simulation results leads to a small descreasing error for lower thicknesses since the assumption (2) on the border effects holds better; fig. 7 shows a comparison for the three considered values of the beam thickness.

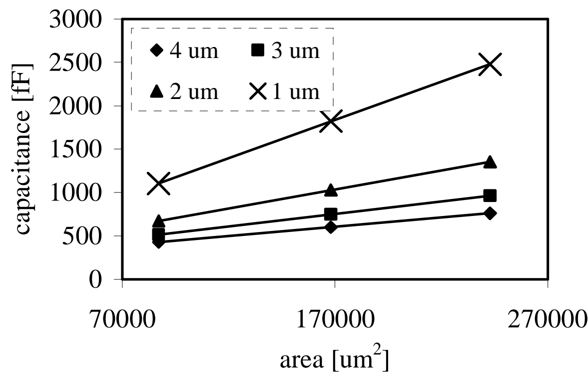

Figure 5 Simulated capacitances for different values of air gap and their linear regression.

	H_S [um]	H_L [um]	W_L[um]	W_S [um]	N_S	T [um]
A1	1.8	0.63	10	290	30	3
A2	1.8	0.63	20	280	30	3
A3	1.8	0.63	30	270	30	3

Table 1 Nominal parameters of the designed test-strucures for air-gap extraction. T is the nominal air-gap.

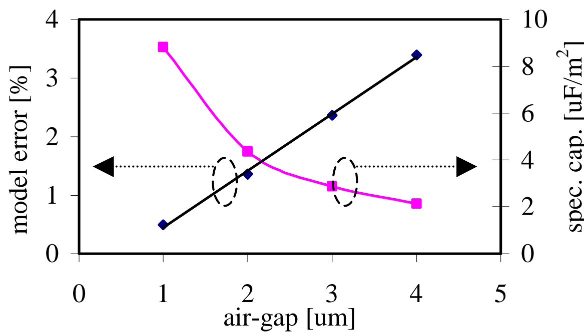

Figure 6 Percentage error introduced by the model vs. air-gap and extracted specific area capacitance.

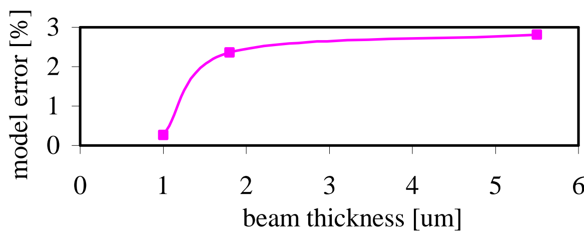

Figure 7 Percentage error introduced by the model vs. beam thickness at the nominal value of the air-gap (3 um).

5. PROFILE ESTIMATION

The introduced methodology on air-gap extraction assumes a flat condition on the suspended beams which usually occurs under the ideal condition of zero-planar residual stress or in tensile regime. Nevertheless, the fabrication process can introduce undesired mechanical deformations that might affect or even dramatically impair the extraction accuracy. A typical issue would be the compressive stress that induces cosine- or arc-shaped deformations [7, 8] or, generally speaking, some uncontrolled fabrication condition that can induce an arbitrary unknown shape. Figure 8 qualitatively shows the buckling effect in presence of compressive stress.

In order to check approximatively if the profiles of the beams are deformed in such a way to impair to overall methodology, an additional set of profiling capacitors can be used. They are identical to the ones in figure 4-a, b, c except for the underneath electrode being split in five parts. Figure 8 shows the cross-section of the profiling capacitor with the largest area in presence of compressive stress. From the five capacitance values, five effective gaps can be extracted together with the approximate profile. An example is shown in figure 9. For obtaining the best check, especially in presence of compressive stress which is sensitive to beam length, all the three profiling capacitors should be used.

The qualitative extracted profile is affected by errors of 20% for displacements over 1.5 um for the nominal air-gap of 3 um. A better model is under investigation.

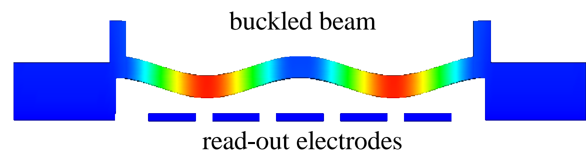

Figure 8 Simulation image of the profiling capacitor with suspended beams affected by compressive residual stress.

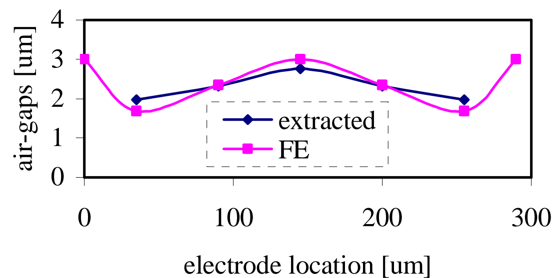

Figure 9 Profile extraction from a profile-capacitor affected by the buckling phenomena.

6. CONCLUSIONS

A methodology for the extraction of dielectric thickness and air-gap by electrical measurements has been shown. The extraction is based on banks of capacitors with variable area and constant perimeter. The methodology is very similar to the one used in microelectronics for unit area capacitances extraction. Its application to the measurement of air-gap in micromachining is not trivial, so a new design strategy has been employed based on a simple electrical model and giving a good extraction accuracy.

The methodology has been experimentally validated for dielectric thickness extraction while for air-gap extraction it has been validated only by FE analysis.

The main source of unreliability of the test-structure for air-gap extraction is a possible mechanical deformation of the suspended beams due to fabrication issues. Non-flatness due to fabrication process can be checked by electrical measurements on a separate set of capacitors in order to decide on the applicability of the methodology.

7. ACKNOWLEDGEMENTS

This work was supported by the MIUR as part of the FIRB project "Enabling Technologies for Wireless Reconfigurable Terminals" (RBNE01F582).

8. REFERENCES

[1] H.A.C. Tilmans, "MEMS components for wireless communication" *Proc. of EUROSENSORS XVI*, Prague, Czech Republic, September 2002, pp. 1-34

[2] N. Abelè et Al., "Comparison of RSG-MOSFET and capacitive MEMS resonator detection", *IEE Electronics Letters*, March 2005, vol. 1, No. 5, pp. 242-244

[3] T. Veijola et Al., "Surface extension model for MEMS squeezed-film dampers" *Proc. of DTIP 2005*, Montreux, CH, June 2005, pp. 405-410

[4] G.M. Rebeiz, *RF MEMS Theory, Design, and Technology*, J. Wiley & Sons Publications, Hoboken, NJ, 2003

[5] P. Nouet et Al., "Use of test structures for characterization and modeling of inter- and intra-layer capacitances in a CMOS process" *IEEE Trans. on Semiconductor Manifacturing*, May 1997, vol. 10, No. 2, pp. 233-241

[6] F.Giacomozzi et Al., "Electromechanical aspects in the optimization of the transmission characteristics of series ohmic RF switches" *Proc. of MEMSWAVE 2004*, Uppsala, Sweden, July 2004, pp. C25-C28

[7] S.D. Senturia, *Microsystem design*, Kluwer Academic Publishers, Norwell, MA, 2001

[8] S.M. Car et Al., "Novel buckled shapes of free-standing mesoscopic beams", *Proc. of 4th IEEE Conf. on Nanotechnology*, München, DE, August 2004, pp. 267-269